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FLASH MEMORY DEVICE AND ARCHITECTURE WITH MULTILEVEL CELLS

ABSTRACT OF THE DISCLOSURE

A FLASH memory has an array of FLASH cells that each store N multiple bits of information as charge stored on a floating gate. Reference voltages or currents are generated for each boundary between the 2^N states or levels and for an upper limit and a lower limit reference for each state. A selected bit line driven by a selected FLASH cell generates a sense node that is compared to a full range of $3*2^N-1$ comparators in parallel. The compare results are decoded to determine which state is read from the selected FLASH cell. An in-range signal is activated when the sense node is between the upper and lower limit references. The target programming count or programming pulses is adjusted during calibration to sense in the middle of the upper and lower limit references. Margin between references is adjusted by calibration codes that select currents for summing.